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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/674,648	CHOE ET AL.	
	Examiner	Art Unit	
	MARIANNE L. PADGETT	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-6,8-11,16-24,27-30,34,39 and 40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-6,8-11,16-24,27-30,34,39 and 40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Applicants' amendment of 9/24/2008 has corrected various 112 first & second problems as set forth in section 2 of the action mailed to 6/25/2008. Specifically, the significant typographical error introduced when claim 40 was first presented, which was directed to immersion in a Hf-containing solution, instead of the disclosed HF-containing solution has been corrected; various range limitations that were broader than the scope of the original disclosure due to the addition of the modifier "about" have been corrected; the limitation concerning the ion implantation of the n- or p-type dopants has been made consistent with the disclosure on [0039] removing new matter, however consistent with the specification, it remains uncertain whether the depth referred to is a range of maximum depths measured from the top of the substrate or a thickness as measured from the top of the substrate starting at 250 nm going down to 1500 nm; and clarifies the porous region oxidative conversion to to clarify the results consistent with the original specification.

2. **Claims 40, 4-6, 8-11, 16-24, 27-30, 34 & 39** are rejected under 35 U.S.C. **112, first** paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 40, 4-6, 8-11, 16-24, 27-30, 34 & 39 are rejected under 35 U.S.C. **112, first** paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Independent claim 40 has been amended to read "the electrolytic anodization process converts **at least a portion** of the activated n-type or p-type dopant region into the porous Si region" (emphasis added), however the examiner finds no indication in the specification that the

activated dopant implanted region (figure 1A, ref.#12 = dopant region, [0039]; figure 1B, ref #14 = activated dopant region, [0042-46]; figure 1C, ref #16 = porous region, [0047-54]) may be only partially converted to porous material, as all teachings appear to indicate that the entire activated dopant region is converted to porous material, thus the claims as amended which do not require conversion of all of the activated dopant region into a porous region would appear to encompass **New Matter**.

As previously indicated on page 4 in section 2 of the action mailed 6/25/2008, the specification as originally filed, as discussed in paragraphs [0040-42+] only provides enablement for implantation of ions select from the group Si, Ge, Ne, Bi, Sn, and Xe, when it is performed before the activation annealing process, thus neither enables nor provide support for claim that encompasses performing this particular ion implantation at times that may be after the activation annealing process, although it is noted that original claims 2 & 31-34 (especially 2 + 31-32) contained uncertain temporal relationships for this ion implantation with respect to the dopant activation step, except that original claim 2's phrasing indicated ion implanting was before dopant activation, but did not positively require that implanting to include the originally claimed "neutral ion" implantation (now more clearly claimed with respect to the above listed elements), so it's presently claimed while not necessarily new matter, thus lack clear enablement.

In the last three lines of claim 40, the amended phrase "... and a remaining portion of the porous silicon region provides a silicon-containing over layer" could be interpreted to mean that part of the porous layer which is over the thermally oxidized buried oxide layer, remains porous, however this is inconsistent with the teachings of the original specification which indicates that the course porous region typically coalesces into monocrystalline silicon & then into a silicon-containing over layer as illustrated in figures 1E & 1F, discussed in [0058], thus this phrasing would appear to encompass possibilities neither taught nor enabled by the original specification,

although also encompasses possibilities that are enabled, i.e. the coalescence, which would appear to indicate that it is no longer porous.

3. **Claims 40, 4-6, 8-11, 16-24, 27-30, 34 & 39** are rejected under 35 U.S.C. **112, second** paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The **claim 40** limitation concerning the ion implantation of the n- or p-type dopants while now consistent with the disclosure on [0039], remains uncertain or ambiguous as to whether the depth referred to is a range of maximum depths measured from the top of the substrate, or if the claim depth represents a thickness as measured from the top of the substrate starting at 250 nm going down to 1500 nm. Note the latter possible interpretation is encompassed by the former interpretation, however either has been considered for purposes of examination over the art, but the scope of the claims acquires clarification on the record

In the last three lines of claim 40, it is uncertain, especially when considered in light of the specification, if this claim is indicating that the silicon-containing over layer is porous, as the wording would suggest that it is or can be, however the specification suggests that it isn't, as discussed above.

4. The **nonstatutory double patenting** rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

The following is a quotation of **35 U.S.C. 103(a)** which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. **Claims 4-6, 8-11, 16-24, 27-30, 34 & 39-40** are rejected under 35 U.S.C. 103(a) as obvious over **Hodge et al.** (5,387,541), in view of **Hiromitsu et al**. (JP 62-245620, English translation) & optionally considering **Bendernagel et al**. (6,800,518 B2).

Applicants' amendment of the independent claim has been amended to not require that all of the activated doped layer is necessarily anodized into a porous region, however the broader amended scope also encompasses the previous limitation thus was covered previously by this rejection.

Applicants' amendment also provides a new requirement that only part of the porous layer becomes the thermally oxidized buried oxide layer, such that there is a silicon containing portion overlying the buried layer which includes a remaining portion of the porous region, however this is unclear in that it is ambiguous whether applicants are requiring it to remain porous or changing it into something else called "a Si-containing over layer", which does not

exclude it remain porous. Note that as applicants requirement that a portion is thermally oxidized and a portion becomes part of the overlying layer (whether or not remains porous), does not indicate what characteristics of the porous region creates any differentiation, what part of a porous region remains porous (are released is not oxidized) & what part is oxidized cannot be clearly determined or treated or considered with respect to this claim limitations as written.

Hodge et al. teach various possible routes for creating a porous layer within the silicon substrate, which may be oxidized so as to form a buried silicon layer. It is noted that in col. 1, lines 35-40, comments concerning the expense & difficulty to control porosity for layers of thickness of less than 0.25 μm (i.e. 250 nm), which value limit & subject would appear to be relevant to the ambiguity noted for the depth of the dopant ion implantation in amended claim 40, since the dopant depth is intricately related to the subsequently created across the location & thickness. Specifically in Hodge et al., see the abstract; figures, noting figure 1 is a flow diagram suggesting various process routes, figure 2 illustrates blanket treatment, while figures 3 & 4 illustrate pattern treatments. Col. 1 discusses known prior art porosity treatments, teaching that dopant level determines number & size of pores (col. 1, lines 8-17), with discussion of porosity levels, such as less than 50% (col. 1, lines 37). The paragraph bridging cols. 1-2 discusses the importance of eliminating nonuniformity, while col. 2, lines 14-31 sets forth the basic process sequence of manufacturing a porous silicon layer in the silicon wafer, then ion implanting into the porous layer causing amorphization therein, followed by recrystallization/annealing, which may provide silicon-on-porous silicon material, that may be considered consistent with the dependent claims 16-17 step of forming a Si-containing cap layer on the substrate after the anodization process. Col. 2, lines 36-68 & col. 5, lines 30-48 discussed electrolytic anodization using hydrofluoric acid (HF), with an exemplary current density of 5.5 mA/cm^2, resulting in porous density of 1.17 g/cm^3 to a depth of 2.6 μm (i.e. >50 nm), with col. 3, lines 1-3 teaching "pre-anodization p+ implant of the non-porous silicon surface and annealed in order to enhance

uniformity of current flow through the wafer during anodization", which is considered to read on ion implanting a dopant (≡ first ion implantation), activation thereof by annealing. Plus it was noted that ion implantation will inherently creating a gradient effect in the porosity, since ion doping will create a gradient concentration of dopant over a range of implantation depths. Any thermal oxidation effects that very dependent on porosity would inherently be created due to such variation, especially considering that porosity as defined by applicant includes what other people would consider approaching theoretical density, i.e. would include overlying silicon substrate areas with minimal implanted dopants, which other people would not have considered to have been made porous, but are porous in light of applicants specification.

In col. 3, lines 4-53 & col.5, lines 49-col. 6, lines 3, after annealing & anodization Hodge et al. teaches ion implantation (≡ second ion implantation) that may include ions, such as **Ge^+, Si^+,** Sn^+, etc., where typical doses are taught to be **$>10^{14}$ ion/cm^2**, used to produce an amorphous layer which may be part of or the entire depth of the porous silicon layer & multiple ion implantations may be employed. While a particular range of ion energies is not taught, an exemplary ion implantation condition of 10^{16} Ge^+/cm^2 at 80 keV followed by 10^{16} F^+/cm^2 at 35 KeV was given, hence while the example is not of an energy in dependent claim 34's range, the particular example would not have been considered limiting by one of ordinary skill of the art, since in order to perform the taught range of various implantation depths that include partial to complete overlap of depth with the porous silicon, one of ordinary skill would reasonably have been expected to adjust their ion energy according to the particular ion & specific depth to which they wish to implant, thus useful Si or Ge ion implantation energies would have been expected to encompass claimed second ion implantation energies, dependent on desired depth & have been determined via routine experimentation. On lines 44-54, note optional use of masking to create amorphous silicon islands on porous silicon surface due to patterned implantation of the equivalent of the second ion implantation.

In col. 3, lines 58-64 & col. 6, lines 4-17 of Hodge et al., see discussion of typical annealing procedures, including preferred alternatives of 3 minutes rapid thermal annealing at 950°C in Ar and also 24 hours at 525°C in nitrogen or argon; col. 3, lines 65-col. 4, line 53 & col. 6, lines 56-col. 7, line 20 for various oxidizing procedures that may be employed when buried oxide layer, i.e. SOI material, is desired to be produced, including possible patterning (col. 4, lines 10-19), a stabilizing oxidation process annealing at 300°C for an hour in flowing oxygen (col. 4, lines 20-31), then a wet oxidation process that uses various sequences or temperatures, including wet oxidation at 800°C for two hours, followed by 1090°C wet oxidation four minutes, where wet oxidations may typically **include gases of H_2 & O_2** (col. 4, lines 32-54), thus encompasses oxygen & hydrogen ambient atmospheres. Applicant's various thermal oxidation & post oxidation steps appear overlap &/or encompass the various possible oxidation steps & sequences as taught by Hodge et al.

Hodge et al. does not explicitly state that the buried oxide layer, which they may produce, is "uniform" nor provide a degree of uniform as in applicants' specification definition, however as basically the same process steps as claimed are employ, the resultant effect would have been expected to be of analogous uniformity, whether one considers that term as a relative term, or within the scope of applicants' 20% thickness uniformity, as combined with defined upper & lower layers, which are consistent with the results of Hodge et al., especially considering their teachings on enhancing uniformity of current flow during anodization, which would have been expected to enhance uniformity of porous layer formation, thus uniformity of resultant buried layer formed therefrom. Alternately, it would've been obvious to one of ordinary skill the art to employ the taught process for making SOI structures so as to make sufficiently uniform, reproducible layers useful for semiconductor device formation. Also see above analogous discussions.

Hodge et al. differs from the new independent claim 40 by not designating a specific depth to which the n-type or p-type dopants used for the anodization/porosity techniques may be implanted, and from dependent claims 4-6 in that while they generically note that in preparation for the anodization process for creating the porosity, p-type dopants may be implanted & annealed, they do not provide any further details of this step, suggesting that one of ordinary skill in the art would have been expected to be conversant with such procedures, such that it would have been obvious for one of ordinary skill in the art to employ techniques known in the art therefore.

The Japanese references to Hiromitsu et al. teach p-type ion implantation into silicon as preparation for creating porous silicon via electrolytic anodization, thus providing details concerning the ion implantation dopant process that one of ordinary skill the art would have expected to be relevant to Hodge et al. Hiromitsu's English abstract is generic with respect to the p-type dopant, but specifically illustrates annealing the ion implanted doped silicon before performing the anodic process in hydrofluoric acid. The translation of Hiromitsu et al. on pages 6-7 indicates B^+ ion implantation (ref. #7) & proton ion implantation (ref. #9, i.e. H+), then annealing at 400°C to form an n-type layer under the nitride pattern (ref #5), where porous silicon (ref #11) is formed by anodization in HF, such that areas with greater density (ref #10) are over areas of lower density in a pattern manner. Hiromitsu et al. discusses neither specific depths of implantation, nor specific thicknesses of implanted regions, or ion energies employed which would be intimately related thereto, however Hiromitsu et al. provides evidence of the known and expected usefulness of B^+ ion implantation for creating the require doped regions for electrolytic anodic creation of porous silicon for use in SOI structure formation as required in the process of Hodge et al., as well as the shown desirability of various configurations relating to density & porosity, hence illustrating the above discussed obviousness for dopants, such as B^+. As previously discussed, dependent claims differ by requiring specific dopants, such as B, instead of

generic teachings of the patent & specific parameters for the implantation, however these would have been obvious variations relevant to routine experimentation & optimization of the process as taught by Hodge et al., in light of prior art suggestions such as those of Hiromitsu et al. and would not be considered to provide patentable significance to the process, as such routine experimentation considerations of the teachings of Hodge et al. would have been expected to encompass such parameters given their teachings that produce analogous results from otherwise like steps.

More specifically with respect to the specifically claimed depth of implantation, or ambiguously bounds of the implantation region & parameters used therefore, while not specifically taught by Hodge et al. (& Hiromitsu et al.), one of ordinary skill in the art would have expected the depth to of been dependent on the particular device requirements, as the anodization technique's creation of porosity is dependent on the present & concentration of dopant, hence depth &/or thickness would have been dependent on where the particular device needed the SOI layer, with optimization of energies & doses following therefrom & determined to be a routine experimentation.

Alternatively, Bendernagel et al. (discussed in previous actions, see sections 10-11 of the action mailed 3/14/2008), who analogously provides SOI structures, supports the above assertions (column 5, lines 28-50 & column 6, lines 28-35) discussing preferred SOI thicknesses of 5 nm-1 μm (referred 5-200 nm) & porous layer thicknesses from anodized doped structures of about 100 nm-2 μm, hence it would've been further obvious to one of ordinary skill in the art to employ such teachings with the process of Hodge et al., including as combined with Hiromitsu et al. for particular dopants, in order to provide guidance on dopant implantation distribution during routine experimentation, while taking into consideration Hodges use of a second ion implanted species to modify the porous layer thickness due to amorphization of the porous layer structure, which thus modifies the resultant SOI layer is thickness, such that claimed depths, dopant ion

energies & doses would have reasonably been expected to be employed in the taught process of the combination dependent on particular device considerations, especially considering suggested desirable porosity & SOI thicknesses Bendernagel et al. would have reasonably been expected to encompass claimed implantation depths. Furthermore, with respect to p-type ion dopant parameters Bendernagel et al. provide guidance of expected effective B concentrations (e.g. dose) for analogous processing, teaching typical values of about 10^{15}-10^{19}, thus providing an obvious basis for routine experimentation for effective values dependent on particular device requirements.

6. **Previous art of interest** was noted to include: the PGPub to Lin (2005/0045984 A1) cited by applicants, is noted to have relevant B ion implantation/anodization/oxidation teachings (abstract; [0014] & [0026]), specifically noting that boron ion doses of 10^{15}-10^{19} atoms/cm^2, creating p-type layers having a thickness of 4000-6000 Angstroms (i.e. 400-600 nm) after implantation & rapid thermal anneal, may be considered to provide cumulative or equivalent teachings & motivations as those provided by Bendernagel et al., with respect to the above rejection.

Zorinsky et al. (4,628,591) is the US version of JP 61-180446 cited by applicants, & is noted to teach the basic process for creating SOI structures via ion implantation using the n-type dopant phosphorus, with subsequent hydrogen fluoride anodization, then oxidation, including use of masking in order to create islands, but does not provide any teachings of specific parameters to employ, expecting one of ordinary skill in the art to be capable of parameter determination.

The English abstracts of Kaneko Shinichiro et al. (JP 62-108539 A) & Mizushina Yoshikiko et al. (JP 56-110247 A), which were cited by applicants in their 6/4/2008 PTO-1449 appear to be too processes that might be a relevant interest, however as there was insufficient detail in the abstracts to determine if they are only of general interest or more, translations were ordered, & having been received are supplied with this action, however these references appear to

be directed to only a single ion implantation associated with relevant anodization & oxidation treatment.

7. **Applicant's arguments** filed 9/24/2008 and discussed above have been fully considered but they are not persuasive.

On page 8 of applicants 9/24/2008 response, applicants discuss that that there is no requirement that a [process] claim recite a sequence, which considered in a vacuum (i.e. not in light of the specification) is literally true, however if applicants' specification only discusses &/or enables a process performed in a particular sequence, while the applicants are not required to claim that sequence, the examiner is required to reject as new matter &/nonenabled any disclosure that is broader than the enabling disclosure &/or not present in the original disclosure, such as performance of taught process steps that are claimed in a scope which encompasses performing them in a sequence not taught.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. **Any inquiry** concerning this communication or earlier communications from the examiner should be directed to **Marianne L. Padgett** whose telephone number is (571) 272-1425. The examiner can normally be reached on M-F from about 9:00 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Meeks, can be reached at (571) 272-1423. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Marianne L. Padgett/
Primary Examiner, Art Unit 1792

MLP/dictation software

1/5/2009